PATENT
8020-1002-1

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of: Yoshiaki HISAMUNE et al.

Appl. No.: **NEW** Group:

Filed: February 27, 2002 Examiner:

For: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE, NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

February 27, 2002

Sir:

The following preliminary amendments and remarks are respectfully submitted in connection with the above-identified application.

IN THE SPECIFICATION:

Page 19, replace third full paragraph as follows:

--Figs. 33A and 33B are a series of cross-sectional views of the conventional nonvolatile semiconductor memory device, illustrating the order of processing steps of the conventional method of manufacturing the conventional nonvolatile semiconductor memory device;--

Page 27, replace last paragraph spanning pages 27 and 28 as follows:

--As described above, by disposing the upper floating gate 24 larger in area size than the lower floating gate 4 on the lower floating gate 4 which is oppositely disposed from the control gate 11 through the floating gate covering insulation film 16, it is possible for the lower floating gate 4 to increase in effect its surface area oppositely disposed from the control gate 11. Consequently, it is also possible to increase a capacitance between the lower floating gate 4 and the control gate 11. Potential of the lower floating gate 4 and the control gate 11 and a capacitance between the lower floating gate 4 and the semiconductor substrate 1. Consequently, it is possible to increase in potential the lower floating gate 4 by increasing the capacitance between the control gate 11 and the lower floating gate 4. As a result, in the second embodiment of the nonvolatile semiconductor memory device of the present invention having the above construction, it is possible to decrease a voltage applied to the control gate 11, which permits a write voltage to be decreased.--

REMARKS

Claims 1-9 are pending in the present application.

Entry of the above amendments is earnestly solicited. An early and favorable first action on the merits is earnestly requested.

Should there be any matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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REL/maf
Attachments

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The third full paragraph on page 19 has been amended as follows:

Figs. 33A[,] and 33B [and 33C] are a series of cross-sectional views of the conventional nonvolatile semiconductor memory device, illustrating the order of processing steps of the conventional method of manufacturing the conventional nonvolatile semiconductor memory device;

The last paragraph on page 27, continuing to page 28, has been amended as follows:

As described above, by disposing the upper floating gate 24 larger in area size than the lower floating gate 4 on the lower floating gate 4 which is oppositely disposed from the control gate 11 through the floating gate covering insulation film 16, it is possible for the lower floating gate 4 to increase in effect its surface area oppositely disposed from the control gate 11. Consequently, it is also possible to increase a capacitance between the lower floating gate 4 and the control gate 11. Potential of the lower floating gate 4 and the control gate 11 and a capacitance between the lower floating gate 4 and the semiconductor substrate 1. Consequently, it is possible to increase in potential the lower floating gate 4 by [incearsing]

increasing the capacitance between the control gate 11 and the lower floating gate 4. As a result, in the second embodiment of the nonvolatile semiconductor memory device of the present invention having the above construction, it is possible to decrease a voltage applied to the control gate 11, which permits a write voltage to be decreased.